AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

Claims 1-21 (Canceled)

22. (Previously Presented) A processor comprising:

a replay system to determine one or more instructions that have not executed properly and to replay the instructions that have not executed properly, said replay system to set an invalid store flag in a storage area if a store instruction has not executed properly;

a memory execution unit coupled to the replay system to execute load and store instructions, wherein if the invalid store flag is set for a store instruction, the replay system is to replay a load instruction that is later in sequence than the invalid store instruction.

23. (Previously Presented) The processor of claim 22 wherein said replay system is to clear said invalid store flag if the store instruction has executed properly.

24. (Previously Presented) The processor of claim 23 wherein said memory execution unit is to replay a plurality of load instructions that are later in sequence than the invalid store instruction while the invalid store flag is set.

25. (Previously Presented) The processor of claim 24 wherein the memory execution unit comprises a memory ordering buffer to maintain an ordering of load and store instructions and a bus queue to handle bus requests to an external bus.

26. (Previously Presented) The processor of claim 24 wherein said replay system comprises a checker to determine whether an instruction has executed properly.

27. (Previously Presented) A processor comprising:

a replay system to determine one or more instructions have not executed properly and to replay the instructions that have not executed properly;

a memory execution unit coupled to the replay system to execute load and store instructions, the memory execution unit including a store buffer including one or more entries for storing information related to store instructions, each entry in the store buffer including an invalid store flag to indicate whether one of said store instructions has executed properly; and

at least one signal line coupled between said replay system and said memory execution unit, said signal line to transmit an external replay signal that is to be generated from the memory execution unit to the replay system if an invalid store flag is set for a store instruction in the store buffer.

28. (Previously Presented) The processor of claim 27 wherein the external replay signal is to be generated for each load instruction that is later in programming sequence than the invalid store instruction, and the replay system is to replay each later in programming sequence load instructions.

29. (Previously Presented) The processor of claim 28 wherein the replay system is to generate an invalid store signal to the memory execution unit over said at least one signal line if

the replay system detects that a store instruction has executed improperly, and the memory execution unit is to the set the invalid store flag for the store instruction in response to the invalid store signal.

30. (Previously Presented) The processor of claim 28 wherein the memory execution unit further comprises a bus queue coupled to the store buffer to issue and track memory requests that are sent to an external bus.

31. (Previously Presented) The processor of claim 30 wherein if there is a store instruction that did not execute properly, the bus queue is to inhibit memory requests to an external bus for load instructions later in programming sequence than the store instruction until the store instruction executes properly.

32. (Previously Presented) A processor comprising:

a replay system to determine one or more instructions that have not executed properly and replaying the instructions that have not executed properly; and

a memory execution unit coupled to the replay system to execute load and store instructions, the memory execution unit including a bus queue to issue and track memory requests to an external bus, the bus queue to be notified by the replay system if a store instruction executes improperly, the bus queue to inhibit memory requests to the external bus for load instructions that are programmatically later in sequence than the store instruction that executed improperly.

33. (Previously Presented) The processor of claim 32 wherein said bus queue is to inhibit said memory requests until the store instruction executes properly.

34. (Previously Presented) The processor of claim 33 wherein the replay system is to generate an invalid store signal to the bus queue in response to detecting that a store instruction has executed improperly.

35. (Previously Presented) The processor of claim 34 wherein the bus queue includes a storage area for an inhibit load flag and the bus queue is to set said inhibit load flag if the bus queue receives the invalid store signal; said bus queue further includes a storage area for a sequence number field to store the sequence number of the store instruction that has executed improperly; said bus queue to inhibit memory requests for later-in-sequence load instructions if the invalid load flag is set.

36. (Previously Presented) A processor comprising:

a replay system to determine one ore more instructions that have not executed properly and to replay those instructions that have not executed properly;

a memory execution unit coupled to the replay system to execute load and store instructions, the memory execution unit including an invalid address flag to indicate whether a store instruction has not executed properly due to an invalid address; wherein if an invalid address flag is set for a store instruction, the replay system is to replay a load instruction having

an address matching the address of the invalid store instruction and that is programmatically later in sequence than the invalid store instruction.

37. (Previously Presented) The processor of claim 36 wherein said replay system is to replay a plurality of load instructions having an address matching the address of the invalid store instruction that is programmatically later in sequence than the invalid store instruction while said invalid address flag is set.

38. (Previously Presented) The processor of claim 37 wherein the memory execution unit includes a storage area for an invalid store flag to indicate if a store instruction has not execute properly and an invalid address flag to indicate whether a store instruction executed improperly due to an invalid data or an invalid address.

39. (Currently Amended) A system comprising:

[[~~A~~]] a memory to store a plurality of instructions;

[[~~A~~]] a processor coupled to said memory and to execute said plurality of instructions; said processor including

a replay system to determine one or more instructions that have not executed properly and to replay the instructions that have not executed properly, said replay system to set an invalid store flag in a storage area if a store instruction has not executed properly;

a memory execution unit coupled to the replay system to execute load and store instructions, wherein if the invalid store flag is set for a store instruction, the replay system is to replay a load instruction that is later in sequence than the invalid store instruction.

40. (Previously Presented) The system of claim 39 wherein said replay system is to clear said invalid store flag if the store instruction has executed properly.

41. (Currently Amended) The system of claim 40 wherein said ~~memory execution unit~~ replay system is to replay a plurality of load instructions that are later in sequence than the invalid store instruction while the invalid store flag is set.

42. (Previously Presented) A system comprising:

a memory to store a plurality of instructions;

a processor coupled to said memory and to execute said plurality of instructions; said processor including

a replay system to determine one or more instructions that have not executed properly and to replay the instructions that have not executed properly;

a memory execution unit coupled to the replay system to execute load and store instructions, the memory execution unit including a store buffer including one or more entries for storing information related to store instructions, each entry in the store buffer including an invalid store flag to indicate whether one of said store instructions has executed properly; and

at least one signal line coupled between said replay system and said memory execution unit, said signal line to transmit an external replay signal that is to be generated from the memory execution unit to the replay system if an invalid store flag is set for a store instruction in the store buffer.

43. (Previously Presented) The system of claim 42 wherein the external replay signal is to be generated for each load instruction that is later in programming sequence than the invalid store instruction, and the replay system is to replay each later in programming sequence load instructions.

44. (Previously Presented) The system of claim 43 wherein the replay system is to generate an invalid store signal to the memory execution unit over said at least one signal line if the replay system detects that a store instruction has executed improperly, and the memory execution unit is to the set the invalid store flag for the store instruction in response to the invalid store signal.

45. (Previously Presented) The system of claim 44 wherein the memory execution unit further comprises a bus queue coupled to the store buffer to issue and track memory requests that are sent to an external bus.

46. (Previously Presented) The system of claim 45 wherein if there is a store instruction that did not execute properly, the bus queue is to inhibit memory requests to an external bus for load instructions later in programming sequence than the store instruction until the store instruction executes properly.